IN THE CLAIMS:

Claims 1-11 (Cancelled)

12. (Currently Amended) A semiconductor device comprising:

an instruction memory for storing an instruction program comprising a plurality of instruction codes as data with an address;

an instruction fetch block for specifying an address in the instruction memory, performing a fetch process for fetching an instruction program read out from the instruction memory, and outputting the plurality of codes;

a decode block for decoding, into a control signal, each of the plurality of instruction codes outputted from the instruction fetch block, and outputting such control signal; and

an extension block for executing an instruction according to a control signal outputted from the decode block, and outputting a conditional-branch-taken signal indicating a status of a conditional branch according to a result of execution of such instruction, wherein when the instruction fetch block performs the fetch process, one of an address which is a branch target address for use when a conditional branch is taken and an address for use when such conditional branch is not taken is selected according to a conditional-branch-taken signal outputted from the execution block, and supplied to the instruction memory, ~~The semiconductor device according to claim 1~~, wherein the instruction memory comprises an X decoder, a Y decoder and a memory array ~~including~~ comprising a plurality of memory cells identified by an output from the X decoder and an output from the Y decoder,

the X decoder having an input address specified by ~~an~~ upper ~~bit~~ bits of a fourth address outputted from the instruction fetch block,

the Y decoder ~~including~~ comprising a normal decoder for decoding ~~a~~ lower ~~bit~~ bits of the fourth address outputted from the instruction fetch block,

a branch Y decoder for decoding ~~a~~ lower ~~bit~~ bits of the branch target address having a same bit width as that of ~~the~~ lower ~~bit~~ bits of the fourth address outputted from the instruction fetch block, and

a selector for receiving an output from the normal Y decoder and an output from the branch Y decoder, selecting one of the outputs according to the conditional-branch-taken signal outputted from the execution block and outputting selected output, wherein the lower ~~bit~~ bits of the fourth address specifying each of the memory cells of the memory array is specified by the output from the selector.

13. (Currently Amended) A semiconductor device comprising:

an instruction memory for storing an instruction program comprising a plurality of instruction codes as data with an address;

an instruction fetch block for specifying an address in the instruction memory, performing a fetch process for fetching an instruction program read out from the instruction memory, and outputting the plurality of codes;

a decode block for decoding, into a control signal, each of the plurality of instruction codes outputted from the instruction fetch block, and outputting such control signal; and

an extension block for executing an instruction according to a control signal outputted from the decode block, and outputting a conditional-branch-taken signal indicating a status of a conditional branch according to a result of execution of such instruction, wherein when the

instruction fetch block performs the fetch process, one of an address which is a branch target address for use when a conditional branch is taken and an address for use when such conditional branch is not taken is selected according to a conditional-branch-taken signal outputted from the execution block, and supplied to the instruction memory, ~~The semiconductor device according to claim 1~~, wherein the instruction memory comprises an X decoder, a Y decoder and a memory array ~~including~~ comprising a plurality of memory cells identified by an output from the X decoder and an output from the Y decoder, the X decoder and the Y decoder each having an input address set by an output from the instruction fetch block, and

the device further comprising a selector for ~~selects~~ selecting the branch target address as input address to the Y decoder based on the conditional-branch-taken signal outputted from the execution block, and outputting the selected address, wherein the branch target address is selected based on a displacement information ~~included~~ in the instruction program data and the fourth address, ~~a~~ lower ~~bit~~ bits of the fourth address specifying each of the memory cells of the memory array is specified by the output from the Y decoder.

14. (Currently Amended) A semiconductor device comprising:

an instruction memory for storing an instruction program comprising a plurality of instruction codes as data with an address;

an instruction fetch block for specifying an address in the instruction memory, performing a fetch process for fetching an instruction program read out from the instruction memory, and outputting the plurality of codes;

a decode block for decoding, into a control signal, each of the plurality of instruction codes outputted from the instruction fetch block, and outputting such control signal; and

an extension block for executing an instruction according to a control signal outputted from the decode block, and outputting a conditional-branch-taken signal indicating a status of a conditional branch according to a result of execution of such instruction, wherein when the instruction fetch block performs the fetch process, one of an address which is a branch target address for use when a conditional branch is taken and an address for use when such conditional branch is not taken is selected according to a conditional-branch-taken signal outputted from the execution block, and supplied to the instruction memory, ~~The semiconductor device according to claim 1~~, wherein the instruction memory comprises an X decoder, a Y decoder and a memory array ~~including~~ comprising a plurality of memory cells identified by an output from the X decoder and an output from the Y decoder,

the X decoder having an input address specified by ~~an~~ upper ~~bit~~ bits of a fourth address outputted from the instruction fetch block,

the Y decoder ~~including~~ comprising a normal Y decoder for decoding ~~a~~ lower ~~bit~~ bits of the fourth address outputted from the instruction fetch block,

a branch Y decoder for decoding ~~a~~ lower ~~bit~~ bits of the branch target address having a same bit width as that of ~~the~~ lower ~~bit~~ bits of the fourth address outputted from the instruction fetch block, and

a selector for receiving an output from the normal Y decoder and an output from the branch Y decoder, selecting one of the outputs according to the conditional-branch-taken signal outputted from the execution block and outputting the selected output, wherein ~~the~~ lower ~~bit~~ bits

of the fourth address specifying each of the memory cells of the memory array is specified by the output from the selector.

15. (Currently Amended) A semiconductor device comprising:

an instruction memory for storing an instruction program comprising a plurality of instruction codes as data with an address;

an instruction fetch block for specifying an address in the instruction memory, performing a fetch process for fetching an instruction program read out from the instruction memory, and outputting the plurality of codes;

a decode block for decoding, into a control signal, each of the plurality of instruction codes outputted from the instruction fetch block, and outputting such control signal; and

an extension block for executing an instruction according to a control signal outputted from the decode block, and outputting a conditional-branch-taken signal indicating a status of a conditional branch according to a result of execution of such instruction, wherein when the instruction fetch block performs the fetch process, one of an address which is a branch target address for use when a conditional branch is taken and an address for use when such conditional branch is not taken is selected according to a conditional-branch-taken signal outputted from the execution block, and supplied to the instruction memory, ~~The semiconductor device according to claim 1~~, wherein the instruction memory comprises an X decoder, a Y decoder and a memory array ~~including~~ comprising a plurality of memory cells identified by an output from the X decoder and an output from the Y decoder, the X decoder and the Y decoder each having an input address set by an output from the instruction fetch block, and

the device further comprising a selector for selecting the branch target address as input address to the Y decoder based on the conditional-branch-taken signal outputted from the execution block, and outputting the selected address, wherein the branch target address is selected based on a displacement information ~~included~~ in the instruction program data and a fourth address, ~~a~~ lower ~~bit~~ bits of the fourth address specifying each of the memory cells of the memory array is specified by the output from the Y decoder.

16. (Currently Amended) A semiconductor device comprising:

an instruction memory for storing an instruction program comprising a plurality of instruction codes as data with an address;

an instruction fetch block for specifying an address in the instruction memory, performing a fetch process for fetching an instruction program read out from the instruction memory, and outputting the plurality of codes;

a decode block for decoding, into a control signal, each of the plurality of instruction codes outputted from the instruction fetch block, and outputting such control signal; and

an extension block for executing an instruction according to a control signal outputted from the decode block, and outputting a conditional-branch-taken signal indicating a status of a conditional branch according to a result of execution of such instruction, wherein when the instruction fetch block performs the fetch process, one of an address which is a branch target address for use when a conditional branch is taken and an address for use when such conditional branch is not taken is selected according to a conditional-branch-taken signal outputted from the execution block, and supplied to the instruction memory, ~~The semiconductor device according to~~

~~claim 1~~, wherein the instruction memory comprises an X decoder, a Y decoder and a memory array ~~including~~ comprising a plurality of memory cells identified by an output from the X decoder and an output from the Y decoder, the X decoder and the Y decoder each having input address set by an output from the instruction fetch block,

the Y decoder selects the branch target address based on a displacement information ~~included~~ in the instruction program data and the output from the fetch process, and outputs the selected address, thereby designating ~~a~~ lower ~~bit~~ bits of the fourth address for specifying each of the memory cells of the memory array, and

the memory array is configured to map a conditional-branch-taken instruction address in each of the instruction codes from the instruction fetch block and a branch target instruction address, so that address inputs to the X decoder become identical and address inputs to the Y decoder alone differ from each other.

17. (Currently Amended) A linking method for performing address mapping for a memory array in a semiconductor device, said semiconductor device comprising:

an instruction memory for storing an instruction program comprising a plurality of instruction codes as data with an address;

an instruction fetch block for specifying an address in the instruction memory, performing a fetch process for fetching an instruction program read out from the instruction memory, and outputting the plurality of codes;

a decode block for decoding, into a control signal, each of the plurality of instruction codes outputted from the instruction fetch block, and outputting such control signal; and

an extension block for executing an instruction according to a control signal outputted from the decode block, and outputting a conditional-branch-taken signal indicating a status of a conditional branch according to a result of execution of such instruction, wherein when the instruction fetch block performs the fetch process, one of an address which is a branch target address for use when a conditional branch is taken and an address for use when such conditional branch is not taken is selected according to a conditional-branch-taken signal outputted from the execution block, and supplied to the instruction memory, ~~The semiconductor device according to claim 1~~, the instruction memory comprising ~~having an instruction memory with~~ a memory array ~~that includes~~ comprising a plurality of memory cells each specified by ~~a~~ upper ~~bit~~ bits and ~~a~~ lower ~~bit~~ bits of a first address, the instruction memory associating, with a second address, an instruction program having a plurality of instruction codes, ~~the~~ upper ~~bit~~ bits and ~~the~~ lower ~~bit~~ bits of the second address being designated in the memory array to perform the instruction program read out from the memory array of the instruction memory, said method comprising:

~~a step of~~ comparing a conditional branch instruction address and a branch target instruction address, each address specifies an instruction program stored in a memory array of an instruction memory,

~~a step of~~ determining whether ~~an~~ upper ~~bit~~ bits of the conditional branch instruction address and the upper ~~bit~~ bits of the branch target address differ, and

~~a step of~~ re-mapping the branch target instruction address so that no carry into ~~the~~ upper ~~bit~~ bits ~~thereof~~ is caused, thereby optimizing arrangements of the conditional branch instruction address and the branch target instruction address, when ~~the~~ upper bits of the conditional branch instruction address and the branch target instruction address differ.